REMARKS/DISCUSSION OF ISSUES

The Applicant thanks Examiner McCarthy for granting an interview on April 23, 2004. The typographical errors in claims 32 and 44 have been corrected. Applicants thank the Examiner for the noted allowance of claims 40 and 43.

Specification. The Applicant has amended the specification herein to correct typographical and format errors. No new matter was introduced by the amendments of the specification herein.

Pending Claims 1-43. In the Non-Final Office Action, Examiner McCarthy rejected pending claims 1-4, 7, 8, 11-14, 17, 18, 21, 22, 24, 26-29, 31-33, 36, 37, 39, 41 and 42 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,978,937 to *Miyamori* et al. The Applicant responds to this rejection as subsequently recited herein, and respectfully requests reconsideration and further examination of the present application under 37 CFR § 1.112.

As to the aforementioned anticipation rejection, the Applicant has thoroughly considered Examiner McCarthy's remarks concerning the patentability of pending claims 1-4, 7, 8, 11-14, 17, 18, 21, 22, 24, 26-29, 31-33, 36, 37, 39, 41 and 42 over *Miyamori*. The Applicant has also thoroughly read *Miyamori*. To warrant this anticipation rejection, *Miyamori* must show each and every limitation of independent claims 1, 11, 21, 26, 36, 39, 41 and 42 in as complete detail as in contained in independent claims 1, 11, 21, 26, 36, 39, 41 and 42. See, MPEP §2131. The Applicant respectfully traverses this anticipation rejection

of independent claims 1, 11, 21, 26, 36, 39, 41 and 42, because *Miyamori* fails to disclose and teaches away from the following limitations of independent claims 1, 11, 21, 26, 36, 39, 41 and 42:

1. "defining a first triggering instruction to provide a first signal to the debugging unit whereby the debugging unit is operable to transition from a first operating state to a second operating state" and "embedding said first triggering instruction within said first set of operating instructions" as recited in independent claim 1;

2. "a processor core operable to fetch an instruction stream including a second signal representative of a first triggering instruction to transition said debugging unit from said first operating state to said second operating state, said processor core further operable to provide said first signal to said debugging unit in response to said second signal" as recited in independent claim 11;

3. "a second computer readable code to transition the debugging unit from a first operating state to a second operating state, said second computer readable code embedded within said first computer readable code" as recited in independent claim 21;

4. "a processor core operable to provide a second signal to the debugging unit in response to said first signal whereby the debugging unit is operable to transition from the first operating state to the second operating state" as recited in independent claim 26;

5. "receiving a first signal representative of a first triggering instruction to transition the debugging unit from a first operating state to a second operating state" as recited in independent claim 36;

6. "receiving a trigger instruction signal representative of a triggering instruction to transition the debugging unit from a first operating state to a second operating state in response to a generation of said first data", and "processing said set of operating signals and said trigger instruction signal to thereby transition the debugging unit from said first operating state to said second operating state in response to a generation of said first data" as recited in independent claim 39;

7. "providing a processor core operable to provide a second signal in response to said first signal" and "providing a debugging unit operable to transition from said first operating state to said second operating state in response to said second signal" as recited in independent claim 41; and

8. "providing a processor core operable to generate said first data or said second data in response to said set of operating signals, and to provide a triggering signal subsequent to a generation of said first data in response to said trigger instruction signal" and "providing a debugging unit operable to transition from said first operating state to said second operating state in response to said triggering signal" as recited in independent claim 42.

As to the traversal, the inventive difference between *Miyamori* and the present invention is that *Miyamori* is conceptually based on a transitioning of a processor core 20 (FIG. 4 of *Miyamori*) between executing a user program stored in a memory 40 (FIG. 4 of *Miyamori*) and executing a distinct debug/monitor program stored in a debugger 60 (FIG. 4 of *Miyamori*), while the present invention is conceptually based on a transitioning of a debugging unit (e.g., unit 30 as shown in FIG. 1 of the present application) between a plurality of operating states (e.g., baseline, dynamic storage and static storage) in response to an execution of a trigger instruction signal generated by a processor core (e.g., core 20 as shown in FIG. 1 of the present application).

As such, *Miyamori* teaches a debug module 30 as an interface between processor core 20 and debugger 60 whereby processor core 20 can download and execute the monitor program when triggered by an interrupt or exception request from the debug module 30 to transition from the normal mode to the debugging mode. See, *Miyamori* at column 2, line 53 to column 4, line 3; and column 5, line 46 to column 7, line 3. *Miyamori* teaches a processor core 20 as having only *one* operating state when triggered by an interrupt or exception request from the debug module 30 to transition from the normal mode to the debugging mode, and that single operating state is to execute the monitor program. *Miyamori* fails to teach any other operating states for processor core 20 by an interrupt or exception request from the debug module 30 to transition from the normal mode to the debugging mode (e.g., to reset itself, to halt the execution of the monitor program or any other debugging program, to logically analyze any debugging data, etc.)

By comparison, the present invention teaches a transitioning of the debugging unit between a plurality of operation states in response to an execution of a triggering instruction signal by a processing core. For example, as illustrated in FIG. 2B of the present application, the present invention teaches (1) a transition of a debugging unit 130 to a baseline operating state in response to a trigger event TE_{S1} that is indicative of an execution of a triggering instruction signal TI_{S1} by a processor core 120, (2) a transition of debugging unit 130 to a

dynamic storage operating state in response to a trigger event TE_{S2} that is indicative of an execution of a triggering instruction signal $T1_{S2}$ by processor core 120, and (13) a transition of debugging unit 130 to a static storage operating state in response to a trigger event TE_{S3} that is indicative of an execution of a triggering instruction signal $T1_{S3}$ by processor core 120.

Withdrawal of the rejection of independent claims 1, 11, 21, 26, 36, 39, 41 and 42 under U.S.C. §102(b) as being anticipated by *Miyamori* is therefore respectfully requested.

Claims 2-4, 7 and 8 depend from independent claim 1. Therefore, dependent claims 2-4, 7 and 8 include all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claims 2-4, 7 and 8 are allowable over *Miyamori* for at least the same reason as set forth herein with respect to independent claim 1 being allowable over *Miyamori*. Moreover, by failing to teach a processor core distinct from a debugging unit and the embedding of a trigger instruction within an instruction stream, the Applicant respectfully asserts that *Miyamori* fails to disclose and teaches away from the limitations of dependent claims 2-4, 7 and 8. Withdrawal of the rejection of dependent claims 2-4, 7 and 8 under U.S.C. §102(b) as being anticipated by *Miyamori* is therefore respectfully requested.

Claims 12-14, 17 and 18 depend from independent claim 11. Therefore, dependent claims 12-14, 17 and 18 include all of the elements and limitations of independent claim 11. It is therefore respectfully submitted by the Applicant that dependent claims 12-14, 17 and 18 are allowable over *Miyamori* for at least the same reason as set forth herein with respect to independent claim 11 being allowable over *Miyamori*. Moreover, by failing to teach a processor core distinct from a debugging unit and the embedding of a trigger instruction within an instruction stream, the Applicant respectfully asserts that *Miyamori* fails to disclose and teaches away from the limitations of dependent claims 12-14, 17 and 18. Withdrawal of the rejection of dependent claims 12-14, 17 and 18 under U.S.C. §102(b) as being anticipated by *Miyamori* is therefore respectfully requested.

Claims 22 and 24 depend from independent claim 21. Therefore, dependent claims 22 and 24 include all of the elements and limitations of independent claim 21. It is therefore respectfully submitted by the Applicant that dependent claims 22 and 24 are allowable over *Miyamori* for at least the same reason as set forth herein with respect to independent claim 21 being allowable over *Miyamori*. Moreover, by failing to teach a processor core distinct from a debugging unit and the embedding of a trigger instruction within an instruction stream, the Applicant respectfully asserts that *Miyamori* fails to disclose and teaches away from the limitations of dependent claims 22 and 24. Withdrawal of the rejection of dependent claims 22 and 24 under U.S.C. §102(b) as being anticipated by *Miyamori* is therefore respectfully requested.

Claims 27-29 and 31-33 depend from independent claim 26. Therefore, dependent claims 27-29 and 31-33 include all of the elements and limitations of independent claim 26. It is therefore respectfully submitted by the Applicant that dependent claims 27-29 and 31-33 are allowable over *Miyamori* for at least the same reason as set forth herein with respect to independent claim 26 being allowable over *Miyamori*. Moreover, by failing to teach a processor core distinct from a debugging unit and the embedding of a trigger instruction within an instruction stream, the Applicant respectfully asserts that *Miyamori* fails to disclose and teaches away from the limitations of dependent claims 27-29 and 31-33. Withdrawal of the rejection of dependent claims 27-29 and 31-33 under U.S.C. §102(b) as being anticipated by *Miyamori* is therefore respectfully requested.

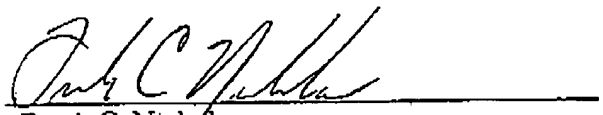
Claim 37 depends from independent claim 36. Therefore, dependent claim 37 includes all of the elements and limitations of independent claim 36. It is therefore respectfully submitted by the Applicant that dependent claim 37 is allowable over *Miyamori* for at least the same reason as set forth herein with respect to independent claim 36 being allowable over *Miyamori*. Moreover, by failing to teach a processor core distinct from a

debugging unit and the embedding of a trigger instruction within an instruction stream, the Applicant respectfully asserts that *Miyamori* fails to disclose and teaches away from the limitations of dependent claim 37. Withdrawal of the rejection of dependent claim 37 under U.S.C. §102(b) as being anticipated by *Miyamori* is therefore respectfully requested.

CONCLUSION

The Applicants respectfully submit that claims 1-43 as listed herein fully satisfy the requirements of 35 U.S.C. §§102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested.

Dated: **May 10, 2004**



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